Source-series-terminated (SST) drivers offer the advantage of providing a large range of termination voltages, making them particularly suitable for multi-standard I/Os [1, 2]. Many standards (e.g., [3]) however, call for larger vertical eye openings that require raising the dc supply voltage from the 1.0V limit for thin-oxide devices in 65nm technology to 1.2 or 1.5V. These requirements are addressed in the proposed SST transmitter design by combining a thin-oxide pre-driver stage running at 1.0V followed by thick-oxide output stages operated at 1.5V. Key features of this design include the implementation of tri-stateable output slices consisting of programmable binary-weighted pre-distortion slices to achieve a mutually independent adjustment of the impedance-tuning and FIR-based transmitter equalization, the level shifter design and the application of T-coils [4] that enable a broad-band impedance matching with a return loss of -16dB over 10GHz bandwidth. Moreover, the transmitter is capable to suppress the clock-duty cycle distortion by a factor of 5x.

Figure 5.7.1 shows a block diagram of the differential half-rate transmitter. The 4b quarter-rate data clocked to the inverter odd post-cursor tap and even post-cursor tap are drivered by two differential current sources. The quarter-rate clock fed to the 4b multiplexer is derived from the global differential CML half-rate clock. The next, the even and odd half-rate clock streams are re-time to the half-rate clock by the retiming stage. The delayed tap of the post-cursor is implemented by two data register latches that are clocked by opposite phases of clock. In the subsequent five parallel blocks used to adjust the FIR weight signals, the even main-tap signal is fed together with the inverted odd post-cursor tap signal to the 1.2 multiplexer in the even data path. Likewise the odd main-tap signal and the inverted even post-cursor tap signal are fed to the 2b multiplexer in the odd data path. The inversion of the post-cursor signals implements the negative sign of the tap weight summation. The outputs of the 2b multiplexers are then retimed again onto the c2-clock and buffered for global distribution to the 22 driver slices.

So far all pre-driver circuits including those of the clock path are implemented with thin-oxide FETs (50nm drawn gate length) at 1.0V dc supply. The actual transmitter output slices however are built with thick-oxide devices (100nm drawn gate length) operated at 1.5V; hence the globally distributed clock and data signals first need to be converted to the higher power supply by means of level shifters. Per output slice, there are one clock level shifter and five data level shifter pairs according to the five tap weights and the even and odd data streams. The two pseudo-differential output drivers per slice, each consist of a pull-up and a pull-down branch implemented as two stacked NMOS or PMOS transistor pairs followed by a polysilicon linearization resistor. The stacked FETs multiplex the half-rate even and odd data streams from the data level shifters into a differential full-rate output. Each of the differential outputs is fed to an impedance-matching Tcoil, where the center-tap is connected to a silicon-controlled-rectifier (SCR)-based ESD protection structure with approximately 3000pf parasitic capacitance. To avoid another power-consuming retiming stage in front of the final output multiplexing, the latency differences between the clock and data path are carefully adjusted by an additional buffer stage at the end of the thin-oxide part of the clock path.

The tap weight summation of the pre-emphasis filter is implicitly performed by the parallel connection of the five binary-weighted pre-emphasis slices. The different slice weights implemented by a binary scaling of the stacked FETs and resistors are denoted by W16 through W7 in the block diagram. Given the five binary weights, the pre-emphasis amplitude resolution is 1/(2^5 - 1).

An important design aspect is that the impedance tuning and the pre-emphasis are orthogonal to each other. The output impedance is determined by the number of parallel connected output slices specified in a configuration register and increases with the number of disabled output slices. As each output slice contains a complete set of tap weights, the pre-emphasis settings can be adjusted without affecting the output impedance of the transmitter. Hence the impedance tuning and the pre-emphasis filtering become independent of each other, greatly simplifying the control logic for impedance and pre-distortion programming.

Key circuit components are the level shifters at the interface between the thin-oxide pre-driver and the thick-oxide output slices because of the timing accuracy and supply-voltage range required. Their basic topology is shown in Fig. 5.7.2. The actual level shifting from 1.0 to 1.5V is performed by the cross-coupled PMOS transistors P3 and P4. To appropriately convert the switching point of the input signal to the corresponding higher level at the output, P3 and P4 have to be dimensioned smaller than the cross-coupled NMOS transistors N3 and N4. This however reduces the capability of P3 and P4 to raise the output at a low-to-high transition sufficiently fast. To solve this inherent problem of level shifting, inverter-like structures consisting of the devices P1, N1 and P2, N2 are connected in parallel to the cross-coupled transistors. These additional circuits constitute a feedback path with respect to the feedback-path-like cross-coupled FETs and thus help pre-bias the outputs such that the cross-coupled PMOS transistors can switch faster despite their smaller size. Care has to be taken that the threshold voltage of P1 and P2 is higher than the amount of voltage level-shifting as otherwise leakage currents will flow at a logical high input.

Test chips implementing 2-channel transmitters with different T-coil and ESD configurations at the outputs are fabricated. Figure 5.7.3 shows a typical eye diagram with -1.9dB pre-emphasis applied to a 7.5Gb/s PRBS-7 signal measured over a measuring section (probes, cables, 3dB attenuator) with 2.5dB loss. The total jitter at a BER of 1E-12 is 16.6ps; 80% thereof is deterministic jitter mainly due to ESD. Figure 5.7.4 shows the measured small-signal small-signal small-signal tests of different transmitter output configurations. Using a T-coil to compensate the parasitic capacitance of the ESD protection results in wideband output-matching and keeps S21 below 10dB up to 14GHz, while occupying 40x40µm². Figure 5.7.5 shows the measured output-versus-clock-duty cycle distortion. Owing to the fully differential clock path using capacitive source-degenerated buffer stages [1], a duty-cycle restoration of 5x is achieved. Figure 5.7.6 shows the de-embedded eye height and the power consumption versus data rate. The differential eye height at the output pins is greater than 1.0V at up to 8.5Gb/s. The die micrograph of a 2-channel transmitter test chip is shown in Figure 5.7.7.

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References:
Figure 5.7.2: Level shifter consisting of thick-oxide FETs used to perform a 1.0V to 1.5V conversion of the clock and data signals.

Figure 5.7.3: Differential eye diagram at 7.5Gb/s with −1.9dB preemphasis measured over a measuring section with 3.5dB loss (probes, 3.5m long cable, 3dB attenuator).

Figure 5.7.4: Measured return loss curves: (a) TX with no ESD and T-coil; (b) TX with SCR used for ESD but no T-coil; (c) TX with SCR and asymmetric T-coil.

Figure 5.7.5: Measured improvement of duty-cycle distortion due to the application of source degenerated buffers in clock path [1]. The duty cycle restoration capability corresponds to a factor of 5x.

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Figure 5.7.5: Measured differential inner eye height (a) without preemphasis and (b) with -1.9dB pre-emphasis; (c) total power consumption composed of (d) driver and (e) clock path contribution.

Figure 5.7.7: Die micrograph of a 2-channel SST TX test chip, where the left TX has a T-coil and a SCR ESD protection at the output, whereas the right TX has neither.